What is claimed is:

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1. A multi-streaming processor comprising:

a plurality of streams for streaming one or more instruction threads;

a set of functional resources for processing instructions from streams; and

a lock mechanism for locking selected memory locations shared by streams of the processor, the hardware-lock mechanism operating to set a lock when an atomic memory sequence is started and to clear a lock when an atomic memory sequence is completed.

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2. The multi-streaming processor of claim 1, wherein the lock mechanism comprises one or more storage locations associated with each stream of the processor, each storage location enabled to store a memory address a lock bit, and a stall bit.

3. The multi-streaming processor of claim 2 wherein, as a stream begins an atomic memory sequence, the targeted memory address is written into the storage location associated with that stream and the lock bit is set, a search of all other storage locations associated with streams is made, and if a memory address match is found with the lock bit set for the matched storage location, the stream sets the stall bit and the stream stalls until the stall bit is cleared.

4. The multi-streaming processor of claim 3 wherein, upon a stream performing an atomic sequence storing the modified result of the sequence to the memory location accessed, the lock bit is cleared in the associated storage location for that stream and all stall bits are cleared in memory

locations associated with streams in the locking mechanism, allowing another stream to begin an atomic sequence.

5. The multi-streaming processor of claim 2 wherein, as a stream begins an atomic memory sequence, the targeted memory address is written into the storage location associated with that stream and the lock bit is set, a search of all other storage locations associated with streams is made, and if a memory address match is not found with the lock bit set for the matched storage location, the stream continues the atomic sequence.

6. The multi-streaming processor of claim 2, wherein the lock mechanism is implemented comprising hardware installed into the multi-streaming processor during manufacturing.

7. The multi-streaming processor of claim 4, wherein the lock mechanism is implemented comprising firmware or software.

8. The multi-streaming processor of claim 2, wherein the storage locations are assigned memory locations in a memory shared by the streams within which the processor performs atomic memory sequences.

9. A method for implementing atomic memory sequences on a multi-streaming processor comprising the steps of:

(a) associating a storage location with each of the streams of the multi-streaming processor, including a lock bit and a stall bit;

(b) upon starting an atomic memory sequence by a stream, writing the memory address to be modified in the sequence into the associated storage location, and setting the lock bit;

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(c) searching all storage locations associated with other streams for memory addresses stored therein, and state of lock bits;

(d) upon finding no match to the memory address having also a set lock bit, continuing the atomic sequence to completion; and

(e) upon finding a match to the memory address with a set lock bit, setting the stall bit for the stream, and stalling operation for the stream until the stall bit is cleared.

10. The method of claim 9 further comprising a step (f) for clearing all stall bits for streams having matching memory address stored in their storage locations upon completion of a store operation at the end of the atomic sequence, thereby allowing another stream to continue with an atomic operation.

11. The method of claim 9, wherein the storage locations are hardware registers implemented on the multi-streaming processor. memory address is located in on-chip memory of the multi-streaming processor.

12. The method of claim 9 wherein the storage locations are reserved locations in the same memory upon which the multi-streaming processor performs atomic memory sequences.